

Application Note 1299

1. Introduction

The Avago Technologies ATF-54143 is a low noise enhancement mode PHEMT designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. Avago Technologies' new enhancement mode technology provides superior performance while allowing a dc grounded source amplifier with a single polarity power supply to be easily designed and built. As opposed to a typical depletion mode PHEMT where the gate must be made negative with respect to the source for proper operation, an enhancement mode PHEMT requires that the gate be made more positive than the source for normal operation. Biasing an enhancement mode PHEMT is much like biasing the typical bipolar junction transistor. Instead of a 0.7 V base to emitter voltage, the enhancement mode PHEMT requires about a 0.6 V potential between the gate and source for nominal drain current.

The ATF-54143 is housed in a 4-lead SC-70 (SOT-343) package. The 800 μm gate width provides lower impedances that are easy to match and a high intercept point.

This application note describes the use of the ATF-54143 in a high dynamic range low noise amplifier designed specifically for base station operating in the 900 MHz cellular frequency band. When biased at a V_{ds} of 4.0 volts and an I_{ds} of 60 mA, the ATF-54143 demonstration amplifier has a nominal 19.5 dB gain, and 0.77 dB noise figure. With some careful optimization of the DC operating condition, an output intercept point of +39 dBm can be achieved. The amplifier has input and output return losses that are better than 12 dB at 900 MHz.

The amplifier is etched on 0.031 inch thickness FR-4 printed circuit board material for low manufacturing costs. The amplifier makes use of low cost miniature multilayer chip inductors for small size.

2. LNA Demoboard

For applications in the VHF through 2.4 GHz frequency range, a generic demonstration board was developed. The board as shown in Figure 1 is etched on 0.031" FR-4 for low cost. The board utilizes small surface mount components. Input and output are via E.F. Johnson SMA connectors part number 142-0701-881.

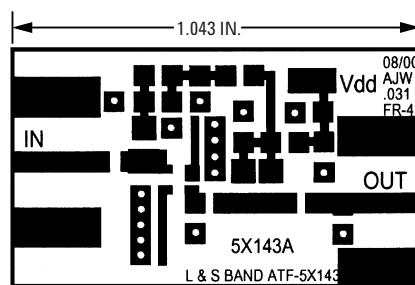


Figure 1. Artwork for the ATF-5X143 series of low noise PHEMT devices

3. Circuit Details

One of the advantages of the enhancement mode PHEMT is the ability to dc ground the source leads and yet require only a single positive polarity power supply. Whereas a depletion mode PHEMT pulls maximum drain current when $V_{gs} = 0$ V, an enhancement mode PHEMT pulls nearly zero drain current when $V_{gs} = 0$ V. The gate must be made positive with respect to the source for the enhancement mode PHEMT to begin pulling drain current. It is also important to note that if the gate terminal is left open circuited, the device will pull some amount of drain current due to leakage current creating a voltage differential between the gate and source terminals.

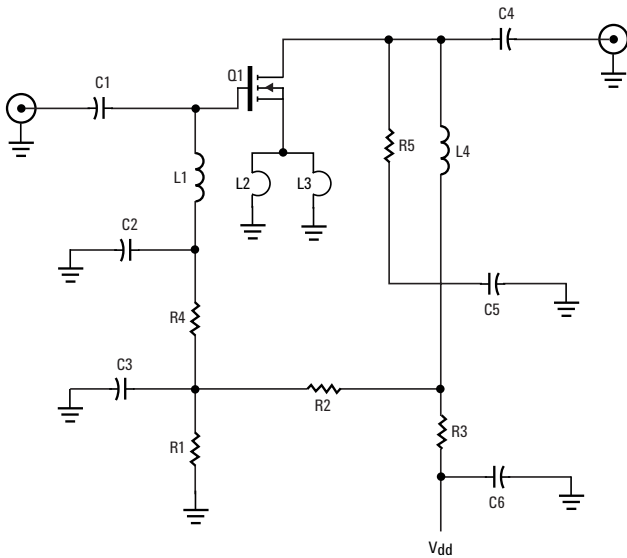


Figure 2. Circuit Diagram

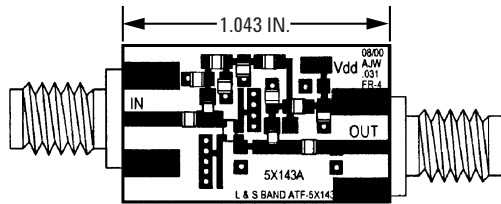


Figure 3. Component placement drawing for the ATF-54143 Low Noise Amplifier

The schematic diagram describing the 900 MHz low noise amplifier is shown in Figure 2. Circuit topology is very similar to the typical depletion mode circuit except for the method of biasing the device. A parts placement drawing is shown in Figure 3. The parts list for the amplifier is shown in Table 1.

Biasing the ATF-54143 is accomplished by the use of a voltage divider consisting of R1 and R2. The voltage for the divider is derived from the drain voltage which provides a form of voltage feedback to help keep drain current constant. While low value resistors in R1 and R2 should improve bias stability, they can result in excessive rectified gate current under large signal input conditions. If the rectified current is not kept below 2 mA, gate metal migration may occur over time. Using the resistor values suggested in Table 1, the rectified gate current, as shown in Figure 4, stays way below 2 mA even at the input power of 10 dBm.

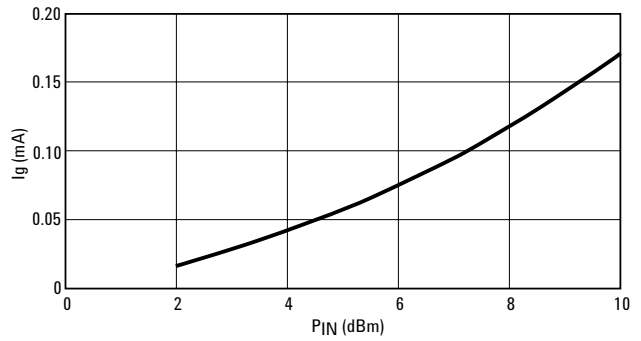


Figure 4. Rectified Gate Current vs. Input Power

Table 1. Parts list for the ATF-54143 amplifier

Part	Value	Qty.
C1, C4	5.6 pF (0805)	2
C2, C5	18 pF (0805)	2
C3, C6	10 nF (0805)	2
L1	6.8 nF (LL2012)	1
L2, L3	Shorting strip	2
L4	8.2 nH (LL2012)	1
R1	4.7 k Ω (0805)	1
R2	33 k Ω (0805)	1
R3	27 Ω (0805)	1
R4	56 Ω (0805)	1
R5	330 Ω (0805)	1
Q1	ATF-54143	1

The purpose of R4 is to enhance the low frequency stability of the device by providing a resistive termination at low frequencies. Capacitor C3 provides a low frequency bypass for R4.

Each source lead is connected to ground through the topside microstrip line etch (LL) and a plated through hole to the bottom ground-plane. The additional inductance LL can have a very pronounced effect on amplifier performance. Some of the effects are undesired, such as out-of-band gain peaking and lower reverse isolation. Beneficial effects include improved input return loss and greater stability. Source inductance is a low loss form of degenerative feedback. It is less noisy in comparison to resistive feedback because there is no feedback resistor to generate thermal noise [1].

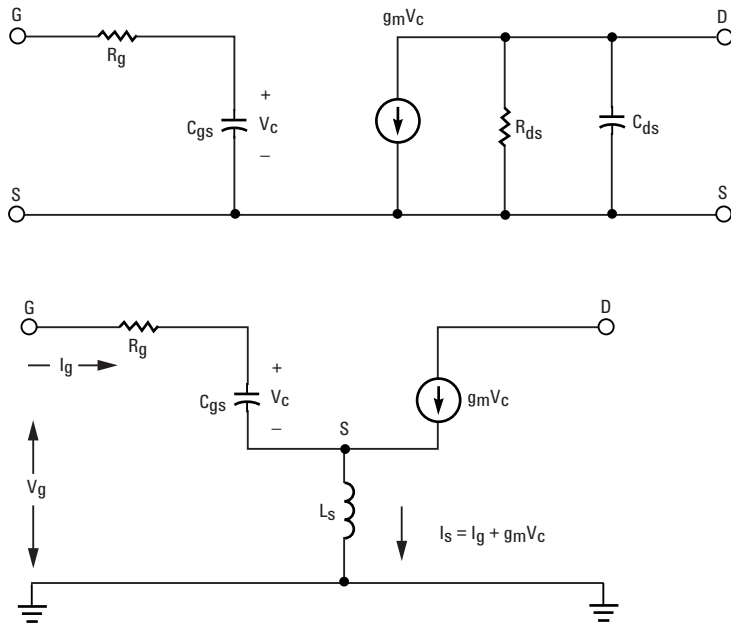


Figure 5. Simplified FET models without source inductance (above) and with external source inductance (below)

Without source feedback, the input impedance of a FET-type transistor can be determined by inspection of the simplified model in Figure 5:

$$Z_{in} = R_g - \frac{1}{j\omega C_{gs}}$$

With the addition of source inductance, the input impedance is modified accordingly [2]:

$$Z_{in}' = R_g + g_m \frac{L_s}{C_{gs}} + j \left[\omega L_s - \frac{1}{\omega C_{gs}} \right]$$

The difference between Z_{in} and

Z_{in}' , indicates that feedback adds

$g_m \frac{L_s}{C_{gs}} + j\omega L_s$ to the input impedance [2].

Generally, the conjugate match (tuning for lowest VSWR) for a RF transistor does not coincide with the optimal noise match (tuning for lowest noise). Therefore, it is very difficult to achieve a low noise figure while maintaining a low input VSWR. The use of source inductance effectively moves the input conjugate match (Γ_{11}^*) closer to the optimal noise match (Γ_{opt}). As more source inductance is being added, the input conjugate match moves along the constant reactance contour [2]. At the same time, Γ_{opt} remains relatively unchanged [3].

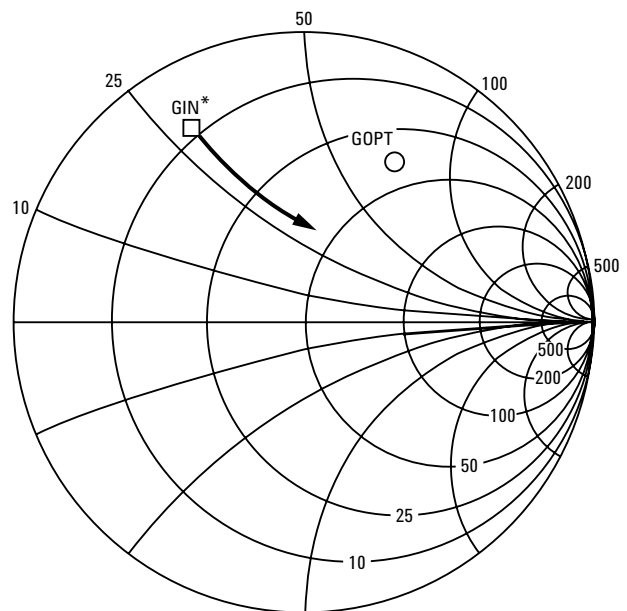


Figure 6. The addition of source inductance shifts the conjugate match closer to the optimal noise match (arrow indicates direction of shift)

The demo board is designed such that the amount of source inductance is variable. Each source lead is connected to a microstrip line, which can be connected to a ground pad at any point along the line. For the amplifier described in this application note, each source lead is connected to its corresponding ground pad at a distance of approximately 2.5 mm (0.1") from the source lead. The distance is measured from the edge of the source lead to the nearest edge of the ground strap (Figure 7). The remaining unused source lead pad should be removed by cutting off the unused etch. On occasion, the unused etch which looks like an open circuited stub has caused high frequency oscillations. During the initial prototype stage, the amount of source inductance can be tuned to optimize performance. More information on the source inductance and its effect on amplifier performance can be found in the Appendix section.

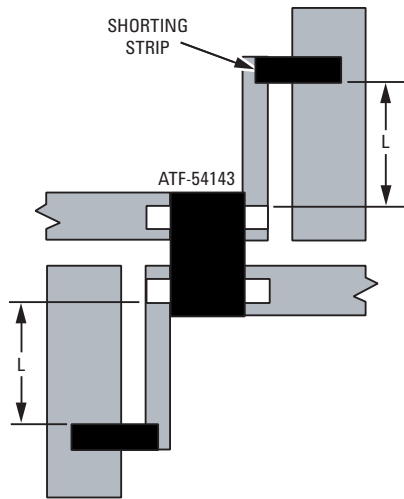


Figure 7. Position of the shorting strips

The amount of source inductance used in the prototype ($L = 2.5 \text{ mm}$, or $0.1''$) was not enough to ensure unconditional stability (e.g. $k > 1$). Unfortunately, further increase in source inductance led to out-of-band gain peaking. To resolve this problem, an output shunt resistor R5 was used to raise the k above one. The output shunt resistor R5 must be chosen carefully as too small a value can lower the intercept point of the amplifier. No excessive gain peaking was noted in the wide-band sweep of Figure 9. Depending on the final layout and component parasitics, circuit stability may be different.

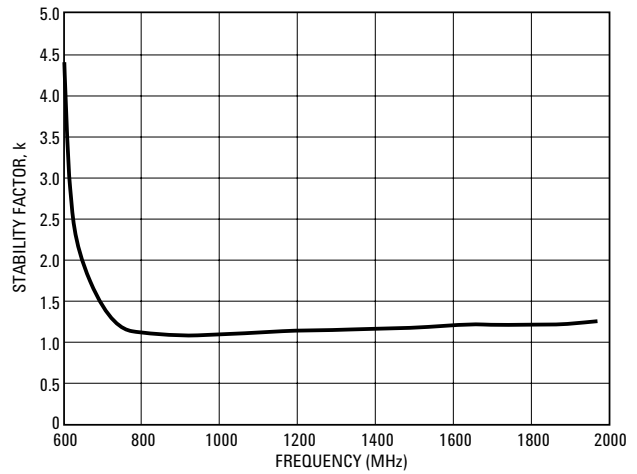


Figure 8. Stability Factor vs. Frequency

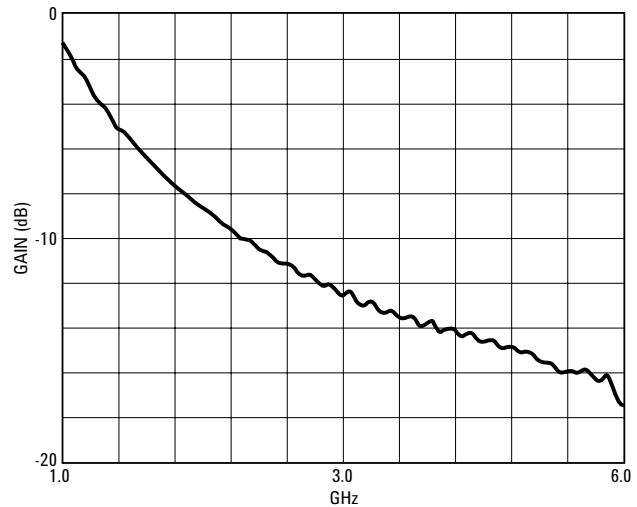


Figure 9. Wide-band gain sweep (1 ~ 6 GHz)

The amplifier uses high-pass impedance matching networks for the input noise match and the output conjugate match. The high-pass network consists of a series capacitor and a shunt inductor. The high-pass topology helps to roll-off the gain below the amplifier's operating frequency, where k is the lowest. The L-section matching networks also double as a means of inserting gate and drain voltages for biasing. Additionally, the series capacitors (C1 and C4) also function as a dc block. The Q of the input shunt inductor (L1) is extremely important from the standpoint of circuit loss and can be calculated from the following equation [4]:

$$\text{loss} = 20 \log \frac{Q_u - Q_l}{Q_u}$$

where Q_u is the unloaded Q-factor of the inductor and Q_l is the loaded Q of the matching network.

Any loss at the input matching network will directly impact the noise figure. Lower element Qs may increase circuit noise figure and should be considered carefully.

At frequencies very much below the amplifier's operating range, the gate is resistively terminated by the combination of R4 and C3. Likewise, R3 and C6 provide a low frequency resistive termination for the drain, which helps stability.

C6 was chosen to be 10,000 pF (or 0.01 μ F) over a 1000 pF capacitor in order to improve output intercept point slightly by terminating the $F_2 - F_1$ difference component of the two test signals used to measure IP_3 . This can be especially important for the IP_3 evaluation when close frequency spacing is used.

4. Performance

The prototype amplifier was tested at a V_{ds} of 4.0 volts and I_d of 60 mA. The measured gain and the noise figure are shown in Figures 10 and 11. The gain measured a nominal 19.5 dB at 900 MHz, while the noise figure was 0.77 dB. The losses in the PCB substrate, matching networks and connectors added to the total noise figure of the amplifier. The low cost FR4 PCB material has made the noise figure somewhat poorer than what could have been achieved using a better substrate.

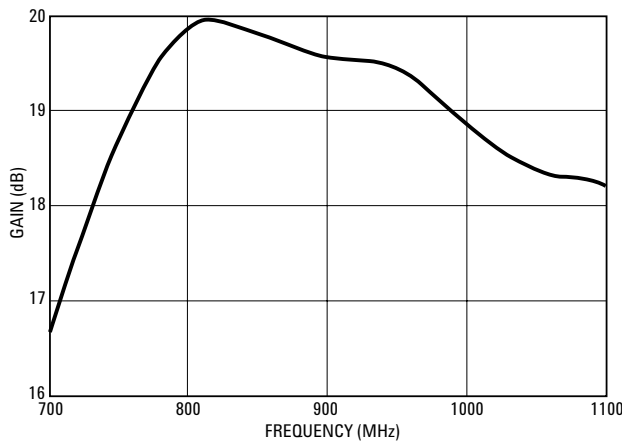


Figure 10. Gain vs. Frequency

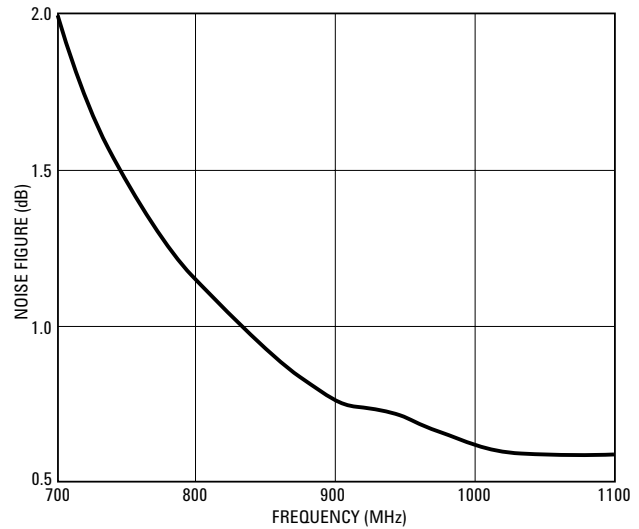


Figure 11. Noise Figure vs. Frequency

The measured input and output return losses are shown in Figure 12. The input and output ports exhibited return losses that were better than 12 dB at 900 MHz. Further improvement in noise figure is possible with some degradation of input return loss by altering the input impedance matching network.

The 1 dB gain compression point, P_{1dB} , indicates the upper limit of the input or output power level at which saturation has started to occur and non-linear effects are becoming increasingly significant. The P_{1dB} is measured by increasing the input power while noting the point when the gain became compressed by 1 dB. This measurement is most commonly referred to the output.

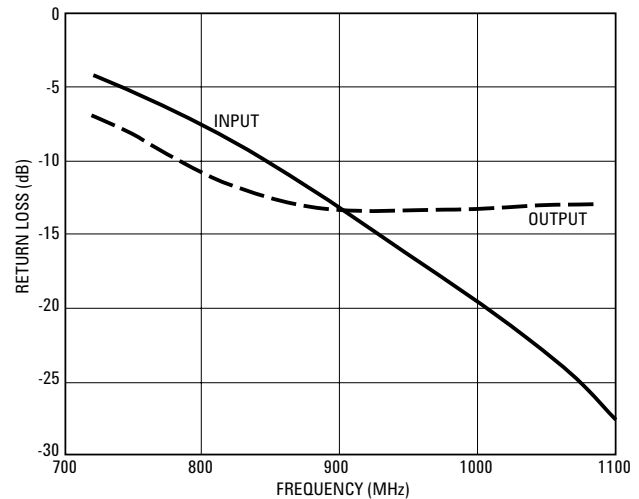


Figure 12. Input and Output Return Losses

The relationship between the gain and the input power is shown in Figure 13. The 1-dB compressed gain (G_{1dB}) and the associated input power (P_{in}) can be read from the graph. The P_{1dB} was calculated as below:

$$P_{1dB} = G_{1dB} + P_{in} = 18.7 - 2.3 = 16.4 \text{ dBm}$$

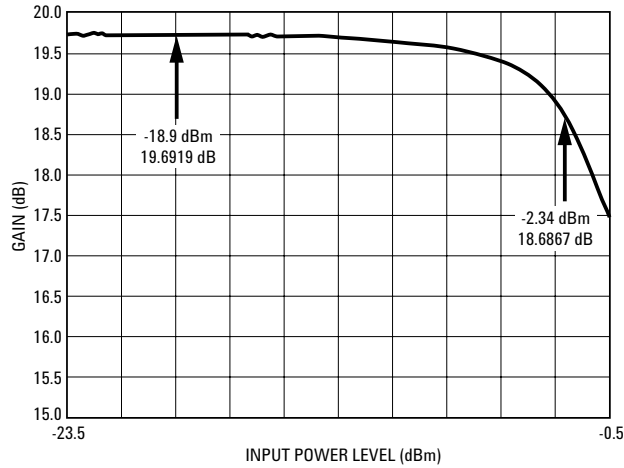


Figure 13. Gain vs. Input Power Level

The intercept point was measured using two test signals with a spacing of 500 kHz. The IP_3 , referred to the output, can be calculated as follows [5]:

$$IP_3 = P_{fund} + \frac{\Delta IM}{2}$$

where P_{fund} is the amplitude of either one of the fundamental output tones, and ΔIM is the amplitude difference between the fundamental tones and the intermodulation products.

The DC operating conditions (V_{ds} and I_{ds}) have a large influence over the IP_3 result. Fixing I_{ds} at 60 mA, Avago Technologies empirically found that the best IP_3 occurred at $V_{ds} = 2.9$ V for the prototype. The third order products were approximately 81.3 dB below the fundamental output tones (Figure 14). Hence, the third-order intercept point, referred to the output, was calculated as below:

$$IP_3 = -0.7 + \frac{81.3}{2} \cong 40.0 \text{ dBm}$$

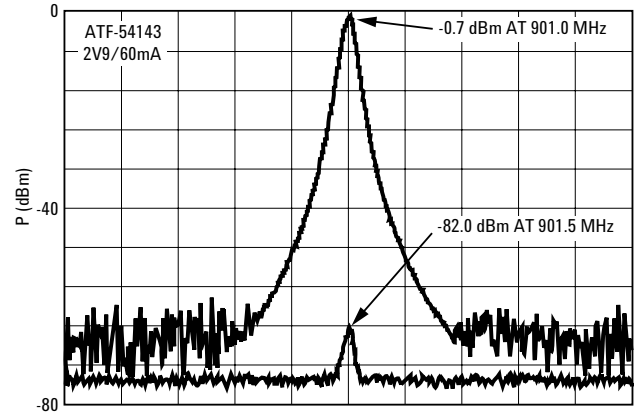


Figure 14. A third order intermodulation product superimposed over one of the two fundamental tones. The two signals were actually separated by 500 kHz.

Based on a nominal gain of 19.5 dB, the corresponding input intercept point (IIP3) was calculated as 20.5 dBm.

5. Appendix:

Determining the Optimum Amount of Source Inductance

Adding additional source inductance has the positive effect of improving input return loss and low frequency stability. A potential down-side is reduced low frequency gain. However, decreased gain also correlates to higher input intercept point. The question then becomes how much source inductance can one add before one has gone too far?

For an amplifier operating in the 2 GHz frequency range, excessive source inductance will usually manifest itself in the form of a gain peak above 6 GHz and even sometimes above 12 GHz. Normally the high frequency amplifier gain roll-off will be gradual and smooth. Adding source inductance begins to add bumps or gain peaks to the once smooth gain roll-off. The source inductance, while having a degenerative effect at low frequencies, is having a regenerative effect at higher frequencies. This shows up as a very high frequency gain peak (S21) and also shows up as input return loss (S11) becoming more positive. Some shift in upper frequency performance is acceptable as long as the amount of source inductance is fixed and has some margin in the design in order to account for S21 variations in the device.

A wide-band gain plot of S21 for an amplifier using the 400-micron gate width ATF-55143 device is shown in Figure 15. The plot shown in Figure 15 represents an amplifier that uses minimal source inductance and has a relatively flat gain response at the higher frequencies. The amplifier has relatively high gain at 2 GHz but less than 0 dB gain above 6 GHz.

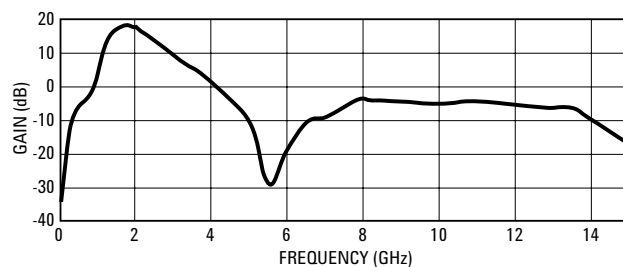


Figure 15. Wide-band gain plot of 2 GHz ATF-55143 amplifier using minimal source inductance

The wideband gain plot shown in Figure 16 is for the same amplifier that uses additional source inductance. Increased source inductance improves low frequency stability by lowering gain at 2 GHz by 1 to 2 dB. Input return loss will also be improved while noise figure will stay relatively constant. The effect of adding additional source inductance can be seen as some gain peaking above 6 GHz. This level of gain peaking shown in Figure 16 is not considered a problem because of its relatively low level compared to the in-band gain.

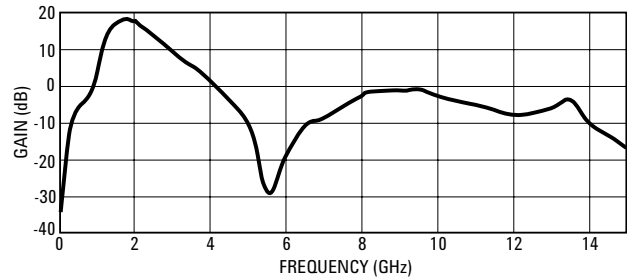


Figure 16. Wide-band gain plot of 2 GHz ATF-55143 amplifier with an acceptable amount of source inductance

Excessive source inductance will cause gain to peak at the higher frequencies and may even cause the input and output return loss to be positive. Adding excessive source inductance will most likely generate a gain peak in the 12 to 13 GHz frequency range which could approach several dB. Its effect can be seen in Figure 17. The end result is poor amplifier stability, especially when the amplifier is placed in a housing with walls and a cover.

Larger gate width devices such as the 800-micron ATF-54143 will be less sensitive to source inductance than the smaller gate width devices and can therefore tolerate more source inductance before instabilities occur. The only drawback of the wider gate width ATF-54143 will be slightly reduced gain. The wide-band gain plot does give the designer a good overall picture as to what to look for when analyzing the effect of excessive source inductance on overall amplifier performance.

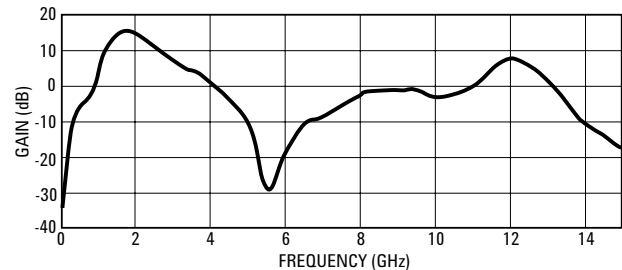


Figure 17. Wide-band gain plot of 2 GHz ATF-55143 amplifier with an unacceptable amount of source inductance producing undesirable gain peaking in the 12 to 13 GHz frequency range

6. References

1. Smith, J., *Modern Communication Circuits*, McGraw-Hill, 1986, chapter 5 sub-topic: Lossless feedback amplifiers.
2. Henkes, D., "LNA Design Uses Series Feedback to Achieve Simultaneous Low Input VSWR and Low Noise", *Applied Microwave & Wireless*, October, 1998.
3. Hewlett-Packard Application Note 1076, "Using the ATF-10236 in Low Noise Amplifier Applications in the UHF through 1.7 GHz Frequency Range", sub-topic: Design Techniques, page 2.
4. Hewlett-Packard Application Note 1085, "900 and 2400 MHz Amplifiers Using the AT-3 Series Low Noise Silicon Bipolar Transistors", page 9.
5. Vizmuller, P., *RF Design Guide*, Artech House, 1995, chapter 3.6: Intercept Point.

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